Session 7 Overview

Non-Volatile Memory

Chair: Giulio Casagrande, STMicroelectronics, Milan, Italy

Associate Chair: Yukihito Oowaki, Toshiba, Kanagawa, Japan

The unprecedented demand for low-cost solid-state non-volatile mass storage to support the growing range of pocket communication/entertainment applications keeps accelerating advances in technology development and design to reduce cost and improve performance. This session reports significant steps forward in cost reduction, by introducing the first 56nm NAND Flash to achieve 8Gb below the 100mm^2 barrier and by showing the first 1Gb NROM packing 4 bits in a single cell. Performance highlights include 10MB/s programming throughput on the 8Gb 2b/cell and a 36MB/s read throughput on a 4Gb 2b/cell obtained by integrating the ECC hardware into the memory chip.

In the mean time, the quest for the Holy Grail memory technology is continuing, and the session shows strong advances on the whole range of emerging technologies, with a paper reporting on a 100MHz Chain FeRAM and two papers reporting on 16Mb MRAM advances in speed and manufacturability. Phase-change memory, the youngest among the emerging memory technologies, is reporting the largest density with a 256Mb chip in 0.1μm technology.

This session opens with a breakthrough paper reporting the first 1Gb NROM storing 4 bits per cell. A 3.5MB/s write throughput is achieved and a V_t distribution-tracking reference scheme is adopted to improve retention and writing endurance.

In Paper 7.2, a 64Mb chain FeRAM with embedded ECC to improve manufacturability and featuring a 200MB/s burst read and write throughput is described.

There are two 16Mb MRAM papers: in Paper 7.3, a circuit technique and a screening methodology that improves manufacturing yield is reported; in Paper 7.4 an array wiring scheme is described that improves array efficiency, and reports a 100MHz synchronous operating frequency.

Phase-change memory is making another leap forward with a 256Mb 1.8V chip in a 0.1μm technology. The PRAM presented in Paper 7.5 shows a write throughput up to 3.3MB/s, comparable to NAND, together with a NOR-like random read access time of 62ns and 66MHz synchronous performance.

In Paper 7.6, for the first time, the integration of an area/performance optimized BCH error detection and correction engine in a 2b/cell 4Gb NAND Flash is shown. It relieves the microcontroller from the burden of performing ECC in software, allowing a record read throughput of 36MB/s after ECC. Up to 5 errors per flexible field are corrected at the cost of only 1.3mm^2 of die area.

The smallest 8Gb NAND ever presented, with a 99mm^2 die size, is reported in Paper 7.7. It is processed on a 56nm technology and achieves an effective bit size of 0.0075μm^2. A write throughput of 10MB/s, the fastest reported for a 2b/cell NAND, is achieved by introducing an 8kB page.

7.1 **A 4b/cell NROM 1Gb Data-Storage Memory** **1:30 PM**
Y. Polansky, Saifun Semiconductors, Netanya, Israel

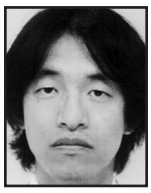
A 4b/cell 1Gb data Flash based on a low-cost NROM process technology is achieved. The design includes a two-phase programming algorithm for supporting a fast and accurate threshold-voltage control. The read scheme incorporates a simple error-detection mechanism combined with an accurate drain-side sensing circuit with a built-in offset cancellation.

7.2 **A 64Mb Chain FeRAM with Quad-BL Architecture and 200MB/s Burst Mode** **2:00 PM**
K. Hoya, Toshiba, Yokohama, Japan

A 64Mb chain FeRAM implemented in 0.13μm 3M CMOS technology is described. A quad-BL architecture reduces the die area by 6.5% and realizes 87.5mm^2 die with an effective cell-size of 0.7191μm^2 while eliminating BL-BL coupling noise. A high-speed ECC circuit and cell data write-back scheme achieves read/write cycle time of 60ns and 200MB/s burst.

7.3 **Signal-Margin-Screening for Multi-Mb MRAM** **2:30 PM**
H. Hönigschmid, Infineon Technologies, Munich, Germany

As MRAM technology is maturing, the need for developing a strategy to identify and replace marginal bits during read/write operation becomes necessary. The methodology and circuit techniques for read/write signal-margin screening implemented in a 0.18μm 16Mb MRAM design, are described. The methodology leads to increased read/write signal margins resulting in fully functional dice by applying a wafer-level screen test including half select disturb pattern.



7.4 **A 16Mb MRAM with FORK Wiring Scheme and Burst Modes** **3:15 PM**
Y. Iwata, Toshiba, Yokohama, Japan

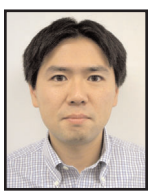
A 16Mb MRAM based on 0.13μm CMOS and 0.24μm MRAM process achieves a 34ns asynchronous access and 100MHz synchronous operation, compatible with pseudo-SRAM for mobile applications. By implementation of FORK wiring scheme, the cell efficiency is raised to 39.9% and the disturb robustness of half-selection state is improved.

7.5 **A 0.1μm 1.8V 256Mb 66MHz Synchronous Burst PRAM** **3:45 PM**
S. Kang, Samsung, Hwasung-City, Korea

A 256Mb PRAM featuring synchronous burst read operation is developed. Using a charge-pump system, write performance is characterized at 1.8V supply. Measured initial read access time and burst-read access time are 62ns and 10ns, respectively. The maximum write throughput is 3.3MB/s.

7.6 **A 4Gb 2b/cell NAND Flash Memory with Embedded 5b BCH ECC for 36MB/s System Read Throughput** **4:15 PM**
R. Micheloni, STMicroelectronics, Agrate Brianza, Italy

A 4Gb 2b/cell NAND Flash memory designed in a 90nm CMOS technology incorporates a 25MHz BCH ECC architecture, correcting up to 5 errors over a flexible data field (1B to 2102B). Two alternative Chien circuits are used depending on the number of errors (1 to 5) thus minimizing latency time. ECC area overhead is less than 1%.



7.7 **A 56nm CMOS 99mm^2 8Gb Multi-level NAND Flash Memory with 10MB/s Program Throughput** **4:45 PM**
K. Takeuchi, Toshiba, Yokohama, Japan

Fabricated in 56nm CMOS technology, an 8Gb multi-level NAND Flash memory occupies 98.8mm^2, with a memory cell size of 0.0075μm^2/b. The 10MB/s programming and 93ms block copy are also realized by introducing 8kB page, noise-cancellation circuits, external page copy and the dual V_{DD} scheme enabling efficient use of 1MB blocks.